

Description of Reference Numerals on the Patent Application Drawings

- 110 bond pad
- 112 dielectric layer
- 114 dielectric layer
- 116 passivation layer
- 118 passivation opening
- 120 portion of the bond pad top surface
- 124 UBM (under bump metallization) layer
- 126 solder bump
- 128 interconnect line
- 130 IC structure
- 210 solder bump
- 212 bond pad
- 214 external contact
- 216 printed circuit board
- 218 underfill material
- 310 Al bond pad
- 312 dielectric layer
- 314 dielectric layer
- 316 interconnect line
- 318 IC structure
- 320 Al bond wire
- 322 bond between wire and pad
- 400 dielectric layer
- 410 dielectric layer
- 412 via plug
- 414 IC structure
- 415 IC structure
- 416 conductive element

- 418 photoresist layer
- 420 etch mask
- 422 etch mask section
- 424 etch mask section
- 426 bond pad hole
- 428 trench
- 429 contiguous opening
- 430 via plug top surface
- 432 barrier/seed layer
- 434 Cu diffusion barrier layer
- 436 Cu seed layer
- 437 cavity
- 438 Cu layer
- 439 metal overcoat layer
- 440 bond pad
- 442 contiguous interconnect line
- 444 passivation layer
- 445 section of Cu layer top surface
- 510 photoresist layer
- 512 hole pattern
- 514 bond pad
- 516 passivation layer
- 518 dielectric layer
- 520 dielectric layer
- 522 IC structure
- 523 metal overcoat layer
- 524 passivation hole
- 526 section of overcoat layer top surface
- 528 top surface of pad overcoat layer
- 529 passivation hole sidewall
- 530 solder bump

532 passivation layer top surface
534 solder bump top portion
610 UBM layer
612 passivation hole
614 passivation layer exposed top surface
616 bond pad
618 passivation layer
620 dielectric layer
622 dielectric layer
624 IC structure
625 metal overcoat layer
626 UBM hole
628 portion of a dielectric layer
630 etch mask
632 UBM
634 portion of UBM
700 UBM layer
710 solder bump
712 passivation layer
713 UBM
714 passivation hole
715 ring shaped UBM portion
716 overcoat layer
718 bond pad
810 via hole
812 via hole
814 bond pad
816 passivation layer
818 dielectric layer
820 dielectric layer
822 conductive element

828 metal overcoat layer
830 Al layer
832 Al via plug
834 Al via plug
836 Al wire bond pad
838 duplex bond pad
910 passivation hole
912 passivation layer
913 section of overcoat layer
916 dielectric layer
918 dielectric layer
920 IC structure
922 bond pad
924 metal overcoat layer
926 Al layer
928 Al plug
930 Al bond pad
932 duplex bond pad
1010 dielectric layer
1012 dielectric layer
1014 IC substrate
1016 conductive element
1018 hole
1020 photoresist layer
1022 etch mask
1024 etch mask section
1026 etch mask section
1028 bond pad hole
1030 trench
1032 contiguous opening
1034 via hole

1036 barrier/seed layer
1037 cavity
1040 Cu layer
1042 metal overcoat layer
1044 via plug
1046 dual damascene structure
1048 bond pad
1050 interconnect line
1051 section of a Cu layer
1052 passivation layer
1054 passivation hole
1056 IC structure
1110 UBM
1112 passivation hole
1114 passivation layer
1116 dielectric layer
1118 dielectric layer
1120 IC substrate
1122 bond pad
1124 metal overcoat layer
1126 Cu layer
1128 barrier/seed layer
1130 solder bump
1210 via hole
1212 via hole
1214 passivation layer
1216 bond pad
1218 metal overcoat layer
1220 Cu layer
1222 barrier/seed layer
1224 dielectric layer

1226 dielectric layer
1228 IC substrate
1310 dielectric layer
1312 dielectric layer
1314 IC structure
1316 conductive element
1318 opening
1320 bond pad hole
1322 trench
1324 via hole
1410 Cu layer
1412 barrier/seed sandwich layer
1414 Cu seed layer
1416 Cu diffusion barrier layer
1418 dielectric layer
1420 dielectric layer
1422 IC structure
1424 via plug
1426 conductive element
1428 cavity
1430 Cu bond pad portion
1431 Cu material
1432 Cu line portion
1433 Cu material
1434 metal overcoat layer
1436 bond pad
1438 contiguous interconnectline
1439 passivation layer
1440 exposed edge
1442 passivation hole
1444 overcoat layer section

1510 UBM
1512 bond pad
1516 metal overcoat layer
1518 barrier/seed sandwich layer
1520 passivation layer
1522 dielectric layer
1524 dielectric layer
1526 IC structure
1610 via hole
1612 via hole
1614 passivation layer
1616 overcoat layer
1618 bond pad
1620 barrier/seed sandwich layer
1622 dielectric layer
1624 dielectric layer
1626 IC structure
1630 Al wire bond pad
1632 via plug
1634 via plug
1636 duplex bond pad
1710 Cu layer
1712 barrier/seed sandwich layer
1714 cavity
1716 dielectric layer
1718 dielectric layer
1720 IC substrate
1722 via hole
1724 conductive element
1726 Cu bond pad portion
1728 Cu interconnect line portion

1729 dual damascene structure
1730 metal overcoat layer
1731 via plug
1732 bond pad
1734 interconnect line
1736 passivation layer
1810 bond pad
1812 dielectric layer
1814 dielectric layer
1816 interconnect line
1818 IC structure
1820 passivation layer
1822 via hole
1824 via hole
1826 via hole
1828 via hole
1830 via hole
1832 solder bump
1833 solder bump plug
1834 solder bump plug
1836 solder bump plug
1910 solder bump
1912 bond pad
1914 solder bump plug
1916 solder bump plug
1918 solder bump plug
1920 passivation layer
1922 metal overcoat layer
1924 Cu layer
1926 dielectric layer
1928 dielectric layer

1930 IC structure
1932 barrier/seed layer
1934 section of Cu layer top surface
2010 Cu bond pad
2012 interconnect line
2014 barrier/seed sandwich layer
2016 dielectric layer
2018 dielectric layer
2020 IC structure
2022 via plug
2024 conductive element
2026 passivation layer
2027 duplex bond pad
2028 Al wire bond pad
2030 via plug
2032 via plug